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After the process in FIG. 2B, as shown in FIG. 6A, a first side wall insulating layer 7a is provided on the side surfaces of the control gate 6 and of the floating gate 4. Then, as shown in FIG. 6B, a resist pattern 1 covering an area on the side of the source region is formed, and the drain region 9 is provided by implanting the ions, i.e., arsenic.

IN THE DRAWINGS:

Applicant respectfully requests approval of two (2) sheets of proposed drawings changes with changes to Figures 1 and 5 shown in red ink. No new matter has been added. A Letter to the Official Draftsperson accompanies this response.

IN THE CLAIMS:

Please replace the text of the claim 2 with the following text:

B5 amd C3

2. The non-volatile semiconductor memory according to claim 1, wherein an impurity dose quantity of said source region is larger than an impurity dose quantity of said drain region.

REMARKS

The Office Action mailed September 21, 2001, has been carefully reviewed and the foregoing amendments and the following remarks are made in response thereto.

As a preliminary matter, Applicant notes the Office Action's acknowledgement of Applicant's election of Group 1, claims 1-6. Applicant also notes the Office Action's indication of non-compliance of the information disclosure statement filed May 8, 2000.

The drawings and the specification stand objected to for minor informalities. Claims 1-6 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 2 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,130,452 to Lu et al. (hereinafter "Lu"). Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu in view of U.S.

Patent No. 5,640,345 to Okuda et al. Claim 5 stands rejected under the same as being unpatentable over Lu in view of the article entitled "A Flash-Erase EEPROM Cell With an Asymmetric Source and Drain Structure" by Kume et al. Claim 6 also stands rejected under the same as being unpatentable over Lu in view of U.S. Patent No. 5,631,179 to Sung et al.

By this amendment, the title, specification and drawings have been amended to address the Examiner's concerns. In particular, the Office Action asserted that the title of the application was not descriptive. Applicant has amended the title to overcome this objection. It is respectfully submitted that the present title is clearly indicative of the invention to which the claims are directed.

The drawings stand objected to for using reference character "7" to designate both the source region and the sidewall spaces in Figure 1 and for not designating Figure 5 by a legend such as –Prior Art--. Applicant respectfully submits in a separate Letter to the Official Draftsperson filed with this response, proposed amendments to Figures 1 and 5 changing reference character "7" to reference character "8" for the source region in Figure 1 and incorporating the legend "Prior Art" in Figure 5. No new matter has been added.

Claim 2 has been amended for clarity. Claims 1 and 3-6 remain unchanged. Thus, claims 1-6 are presently pending in this application for consideration.

Applicant respectfully submits that the pending claims are patentably distinguishable over the cited references as required by § 102 and §103. Applicant further submits that the cited references, whether taken alone or in any combination, fail to disclose (1) hot electrons generated in the vicinity of the drain region and implanted into the electric charge accumulating portion and (2) an overlap of a drain region with the electric charge accumulating portion is set larger than an overlap of the source region with the electric charge accumulating portion as recited in independent claim 1. Thus, claim 1 and all claims dependent therefrom are allowable over the cited references. These distinctions will be further described in the following sections.

THE CLAIMS COMPLY WITH 35 U.S.C. § 112, FIRST AND SECOND PARAGRAPHS

Claim 2 stands rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully submits that claim 2 has been amended for clarity and now complies with the requirements of 35 U.S.C. § 112, second paragraph.

Claims 1-6 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, the Examiner asserts that there is no support for the source region introduced by an impurity, self-aligned with a side wall provided in the control gate as recited in claim 1 and the source region introduced by an impurity, self-aligned by a dual layer side wall as recited in claim 6.

Applicant respectfully submits that the claimed subject matter was described in the specification is such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Page 8, lines 4-16, for example, clearly state that and n^+ type source region 8 is formed by an ion implantation in a self-aligning manner with a left side surface of the side wall insulating layer 7. In addition, the source region 8 overlaps the floating gate 4 due to an impurity rediffusion by a thermal treatment after implanting the ions. The source region thus takes an asymmetric structure corresponding to an existence or non-existence of the side wall insulating layer 7 during the ion implantation process. Page 8, lines 4-16 of the present specification also clearly describe an n^+ drain region formed by an ion implantation in a self-aligning manner with a right edge of a control gate 6. The drain region 9 also overlaps the floating gate 4 due to the impurity rediffusion by the thermal treatment after implanting the ions.

Thus, given the written description, one skilled in the art would understand that the source is made by introducing an impurity in self-alignment with a side wall provided on the side surface of the control gate as recited in claim 1. Furthermore, given the written description, one skilled in the art would understand that the drain region is formed in self-

alignment with a first side wall and the source region is formed in self-alignment with the second side wall as recited in claim 6.

Accordingly, Applicant respectfully submits that one skilled in the art could make and use the present invention given the existing specification and this rejection should be withdrawn.

THE CLAIMS DISTINGUISH OVER THE CITED REFERENCES

Claim 1-3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Lu. These rejections are respectfully traversed since independent claim 1 includes the feature of hot electrons generated in the vicinity of the drain region and implanted into the electric charge accumulating portion and the arrangement of an overlap of a drain region with the electric charge accumulating portion is set larger than an overlap of the source region with the electric charge accumulating portion. This claimed feature and claimed arrangement are not disclosed or suggested in Lu.

The present invention is directed to a semiconductor device having a memory cell structure with a decreased a gate length but maintaining an effective channel length. According to one embodiment of the present invention, the semiconductor device includes a substrate, a control gate, a source region provided by introducing an impurity in a self-aligning manner with a side wall provided on a side surface of the control gate, a drain region and an electric charge accumulating portion. The semiconductor device performs its write operation by generating hot electrons in the vicinity of the drain region and injecting the hot electrons into the electric charge accumulating portion. The semiconductor device is arranged such that the overlap of the drain region with the electric charge accumulating portion is set larger than the overlap of the source region with the electric charge accumulating portion. With this arrangement, it is possible to reduce the gate length while ensuring an effective channel length that is required for the proper operation of the semiconductor device (See, Specification, page 4, lines 5-18 and page 8, lines 24-36). Lu fails to disclose or suggest this claimed feature and arrangement.

Lu is directed to a non-volatile semiconductor device having an asymmetrically placed source and drain. As an initial matter, Applicant would like to point out the semiconductor device disclosed in Lu is totally different from the semiconductor device of

the present invention. The device in Lu requires the used of Fowler-Nordheim (FN) tunneling for writing in erasing operations compared with the present invention, which requires the use of hot electron injection for its writing and erasing operations. These semiconductor devices operate in totally different ways. Thus, Lu fails to disclose hot electrons generated in the vicinity of the drain region and implanted into the electric charge accumulating portion as claimed.

Moreover, Lu fails to disclose the arrangement of the overlap of the drain region with the electric charge accumulating portion is set larger than the overlap of the source region with the electric charge accumulating portion. Lu merely provides the positional relationship between the gate and the diffusion layers. There is no teaching or suggestion of the overlap of the gate and drain region where hot electron injection takes place being greater than the overlap of the gate and source region where hot electron injection doesn't take place.

In view of the absence of the above claimed feature and claimed arrangement, Lu cannot be said to anticipate and does not render obvious the apparatus defined by claim 1. Moreover, since claim 1 is allowable, the claims dependent therefrom, namely claims 2-6 are also allowable. Further remarks regarding the asserted relationship between these claims and the cited references are not necessary in view of their allowability. Applicant's silence as to the Examiner's comments is not indicative of an acquiescence to the stated grounds of rejection.

CONCLUSION

In view of the foregoing remarks, the Applicant respectfully submits that this application is in condition for allowance and request early notice to that effect.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Washington, D.C. telephone number 202 637-3615 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

HOGAN & HARTSON, L.L.P

Date: 3/22/02

By: _____

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Version with markings to show changes made:

IN THE SPECIFICATION:

Please amend the paragraph on page 4, starting at line 5 as follows:

The memory cell according to the present invention, the edge of the source region on the side of the channel region is defined by the side wall insulating layer of the control gate, and the edge of the drain region on the side of the channel region is defined by the edge of the control gate or by the outer side of the thin side wall insulating layer [o] or the side surface of the control gate. Accordingly, there is obtained an asymmetric memory cell structure, in which the overlap of the source region with the electric charge accumulating portion (typified by the floating gate) is set to the minimum necessary enough to cause no offset, and the overlap of the drain region with the floating gate is set larger than that of the source region. It is therefore possible to reduce a gate length while ensuring an effective channel length required.

Please amend the paragraph on page 9, starting at line 26 as follows:

Thereafter, an oxide layer 13 is provided on exposed surfaces of the control gate 6 and of floating gate 4 and on the surface of the substrate 1 by effecting the thermal oxidation. As shown in FIG. 2C, a resist pattern 11 covering an area on the source region side is thereafter provided by the lithography process. Then, the ion, i.e., arsenic is implanted, thereby providing the n^+ type drain region 9 self-aligned with the control gate 6. At this stage, however, the impurity in the drain region 9 is not yet activated. The dose quantity of arsenic is set on the order of, e.g., [2E15] $2 \times 10^{15}/cm^2$.

Please amend the paragraph on page 10, starting at line 4 as follows:

Next, the lithography process is again executed, thereby providing a resist pattern 12 covering an area on the side of the drain region 9 as shown in FIG. 2E. Then, the ion, i.e., arsenic, is implanted, thereby providing the n^+ type source region 8 self-aligned with the side wall insulating layer 7. At that time the dose quantity of arsenic is set on the order of, e.g., [5E15] $5 \times 10^{15}/cm^2$.

Please amend the paragraph on page 15, starting at line 3 as follows:

After the process in FIG. 2B, as shown in FIG. 6A, a first side wall insulating layer 7a is provided on the side surfaces of the control gate 6 and of the floating gate 4. Then, as shown in FIG. 6B, a resist pattern 1 covering [ana res] an area on the side of the source region is formed, and the drain region 9 is provided by implanting the ions, i.e., arsenic.

IN THE CLAIMS:

Please amend the claims as follows:

2. (Once Amended) The non-volatile semiconductor memory according to claim 1, wherein an [said] impurity dose quantity of said source region is larger than an impurity dose quantity of said drain region.